A 9.15mW 0.22mm^2 10b 204MS/s Pipelined SAR ADC in 65nm CMOS

Young-Deuk Jeon[1], Young-Kyun Cho[1], Jae-Won Nam[1], Kwi-Dong Kim[1],
Woo-Yol Lee[2], Kuk-Tae Hong[2], and Jong-Kee Kwon[1]

[1]Electronics and Telecommunications Research Institute
[2]LG Electronics

***Abstract*-This paper describes a 10b 204MS/s analog-to-digital converter (ADC) employing a pipelined successive approximation register (SAR) architecture for low power consumption and small area. To improve the operation frequency, the pipelined SAR ADC consists of two channels with a proposed asynchronous timing technique. This technique increases the amplification time of a residue opamp. To reduce power and area, the opamp is shared between two channels. A reference buffer with a deglitch circuit reduces the glitch and settling time of reference voltages. The prototype ADC fabricated in a 65nm CMOS process shows a SNDR of 55.2dB and a SFDR of 63.5dB with a 2.4MHz input at 204MS/s. The ADC occupies 0.22mm^2 and dissipates 9.15mW at a 1.0V supply. The FoM of the ADC is 95.4fJ/conversion-step.**

I. Introduction

Recently, as the requirement of digital TV is rapidly increased, low-power small-area 10b analog-to-digital converters (ADCs) with 165MHz sampling rate or higher are considered to be one of the significant components. To satisfy the specification in this application, pipelined ADCs are typically used to optimize the power and area [1]-[3]. On the other hand, with the scaling down of CMOS technology, successive approximation register (SAR) ADCs have been replacing pipelined ADCs due to their high power efficiency [4]-[5]. However, the operation speed of SAR ADCs is limited to less than 100MS/s at a 10-bit resolution due to its iteration operations, although high-speed design techniques and calibration schemes are adopted. Moreover, the input sampling time is shorter than 20% of an input clock period to obtain the sufficient SAR conversion time [5]. It increases the power and size of a buffer driving SAR ADCs. Another design issue is trade-off between the number of unit capacitor and the total sampling capacitance. In high resolution SAR ADCs, the total sampling capacitance is often larger than the capacitance considering the kT/C noise because the number of unit capacitor is exponentially increased according to the resolution. So, the methods reducing the number and the size of unit capacitor have been researched.

One method to overcome these issues are to apply a pipeline architecture to the SAR ADCs [6],[7]. The pipelined SAR ADC converts the analog signal to digital codes by stage such as conventional pipelined ADCs. The SAR conversion time is decreased since each stage requires low resolution SAR ADC under 5~6 bits. However, this architecture needs 3-phase timing with input sampling, SAR conversion, and amplification. The input sampling and amplification times of the conventional pipelined SAR ADCs are shorter than half of the operation period. Also, in some case, two or more SAR conversions are occurred in the same phase. It requires the reference buffer with large current driving ability to obtain the required resolution.

In this work, a proposed 10b 204MS/s pipelined SAR ADC with low power consumption and small chip area is presented. The operation speed of the proposed ADC is improved by a dual-channel structure based on an opamp sharing. The amplification time of the residue opamp is increased by a proposed asynchronous timing technique. An internal reference buffer with a proposed deglitch circuit controlling the dynamic current reduces reference voltage variations and improves the ADC performance.

II. Proposed ADC Architecture

A. Pipelined SAR Architecture with Dual Channel

Fig. 1 shows the architecture of the proposed 10b 204MS/s pipelined SAR ADC operating at a 1.0V supply. The ADC consists of channel1(ch1) and channel2(ch2) with common blocks such as an error correction logic (ECL), two reference buffers with a deglitch circuit, a current generator and a 4-phase clock generator. In each channel, sub-ADCs are implemented with the 4b and the 7b SAR ADCs and an analog input signal is sequentially processed in two steps, as in pipelined ADCs. A C-array1 and a C-array2 have a binary-weighted capacitor and a bridge capacitor architectures to optimize the die area, respectively. The function of a residue

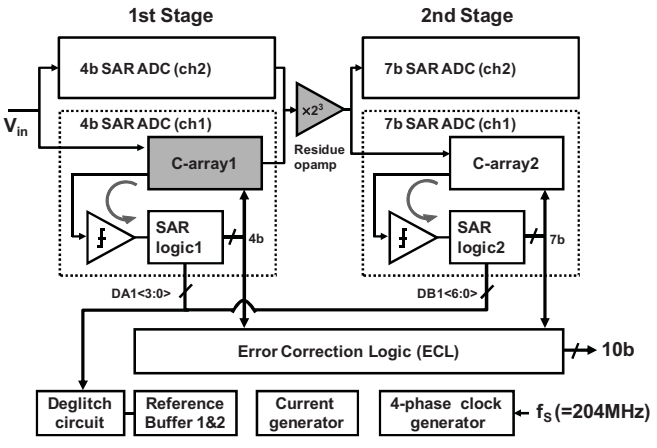

Fig. 1. Architecture of the proposed 10b 204MS/s SAR ADC.

978-1-4244-5760-1/10/$26.00 ©2010 IEEE

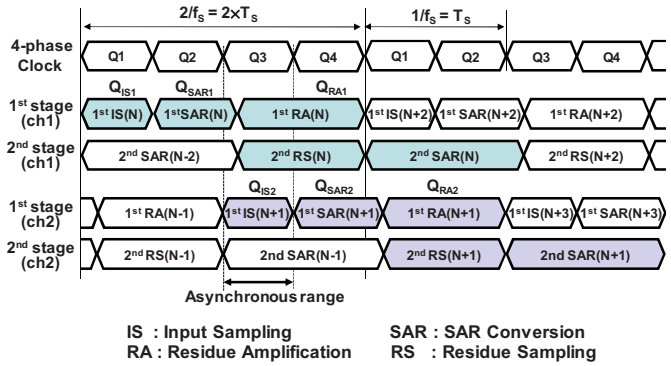

Fig. 2 Proposed ADC operation using an asynchronous timing technique.

amplification is performed by a residue opamp sharing two C-array1 in the first stage. The ECL corrects the digital codes by overlapping one bit between the first and the second stages. The reference buffers with the proposed deglitch circuit reduce the fluctuation of the reference voltages using the dynamic current. The current generator used instead of a BGR adopts a modified Widlar current source for a low supply voltage and a small area. The clock circuit generates a 4-phase clock with a half of the input clock frequency to drive the pipelined SAR ADC.

B. Pipelined SAR ADC Operation

The proposed ADC operation using an asynchronous timing technique is illustrated in Fig. 2. The asynchronous clocks of Q_{IS}, Q_{SAR}, and Q_{RA} based on the 4-phase clock are generated by internal asynchronous clock circuits in the first stage and the second stages. First, the ADC operation of the channel1 is as follows. In Q1 phase identical to Q_{IS1}, the analog input signal is sampled on the C-array1 of the first stage. At the same time, the 7b SAR ADC in the second stage converts the previous analog input to 7b digital codes. When Q1 is low, the 4b SAR conversion in the first stage is started. The one-bit decision time in the SAR ADC is less than 0.8ns. At the instance of both the first and the second SAR ADC conversions are complete, Q_{SAR} falls low and Q_{RA} rises high, automatically. The rising point of Q_{RA} is limited within Q3 phase to share the residue opamp. Then, the residue opamp amplifies the difference between the analog input and the 4b digital code and transfers the residue voltage to the second stage. The 7b SAR ADC conversion is started in the rising edge of subsequent Q1.

As shown in Fig.2, the period of the input sampling clock, Q_{IS}, is fixed to $T_S/2$ and the periods of Q_{SAR} and Q_{RA} are allowed to vary. Therefore, the Q_{RA} period becomes $2\times T_S$-$T_S/2$-T_{SAR}, which is approximately 4.15ns at a 204MHz sampling frequency. The sampling period is maintained and the amplification time is increased compared to those of conventional pipelined ADCs. If the proposed asynchronous timing technique is applied to the single-channel pipelined SAR ADC operating at low sampling frequency, the falling edge of Q_{SAR} is in Q2 phase and the Q_{RA} period can be increased by more than half of the cycle. In this case, the power consumption and die size of the pipelined SAR ADC can be significantly reduced.

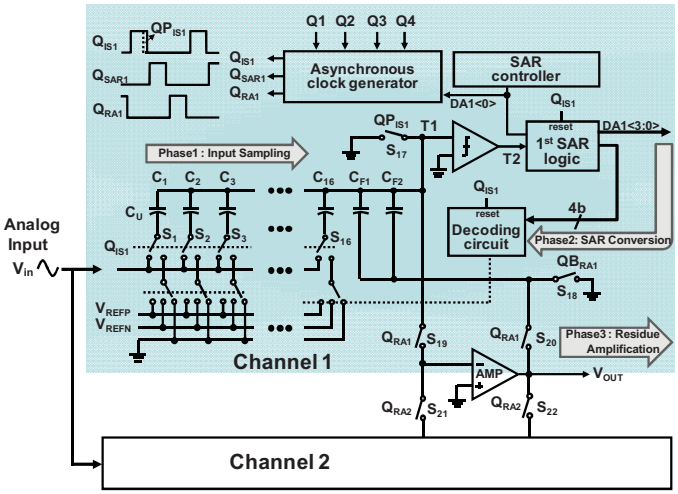

Fig. 3 First stage with a SAR ADC and a residue opamp.

The ADC operation of the channel 2 is identical to that of channel 1 except for Q3 input sampling. Because the RA periods of the channel1 and channel2 are not overlapped, the residue opamp can be shared. Each channel is independently operated with a 102MS/s and the proposed ADC has throughput of the 204MS/s.

III. Circuit Implementation

A. First Stage with SAR ADC and Residue Opamp

Fig. 3 shows the block diagram of the first stage. The channel1 is described in upper blocks and the channel2 is the same with the channel1 except for the asynchronous clock phases. In the channel1, the 4b SAR ADC is composed of the C-array1 with 16 unit capacitors, a comparator, a SAR logic, a decoding circuit, and a SAR controller. The C-array1 connected to the comparator and the opamp is used in the input sampling, the SAR conversion, and the residue amplification phases. As a result, an input sampling mismatch does not occur and a front-end S/H is not needed. Also, it decreases the chip area of the ADC because the SAR function block without C-array1 can be implemented by logic circuits. Switches S_{19}~S_{22} are added to share the opamp between the channel1 and the channel2. To reduce the parasitic capacitance of T1 node, the capacitors using the metal-oxide-metal (MOM) structure are implemented with the metal layers 2 to 5. The unit capacitance and the total sampling capacitance of the C-array1 are 100fF and 1.6pF considering capacitor matching and kT/C noise, respectively. The comparator is composed of a preamp and a latch. The thermal noise of the comparator is nearly ignored due to its low resolution. The SAR controller generates the internal clock for SAR iteration operation to eliminate the necessity for an external high-speed clock. The bit-decision signals, DA1<3:0>, are generated by the SAR logic whenever the 4b SAR ADC successively determines the digital codes. The asynchronous clocks of Q_{IS}, Q_{SAR}, and Q_{RA} are made by a combination of the 4-phase clock and the bit-decision signal, DA1<0> for the proposed asynchronous timing technique.

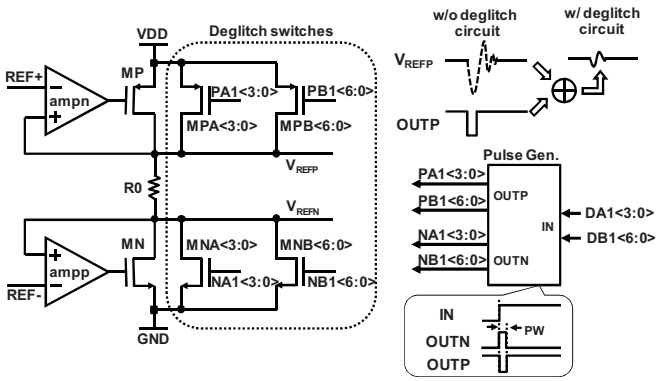

Fig. 4 Reference buffer with the deglitch circuit.

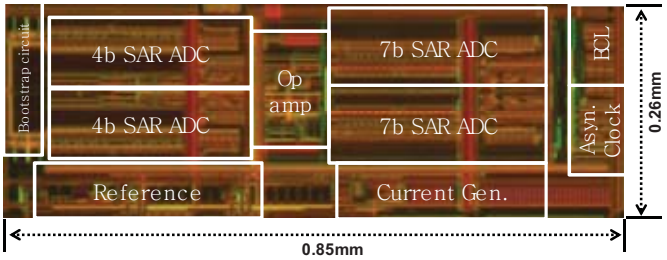

Fig. 5 Chip photograph.

The operation of the first stage is explained by three phases of input sampling, SAR conversion, and residue amplification. In the input sampling phase, the analog input signal is sampled on unit capacitors C_1 to C_{16} through the bootstrapped NMOS switches S_1 to S_{16} to improve the linearity of the input signal. The bottom plates of feedback capacitors C_{F1} and C_{F2} and the T1 node are connected to GND. At the same time, the first SAR logic and the decoding circuit are reset to their initial conditions. When Q_{IS} is low, the bottom plates of the capacitors C_1 to C_{16} are connected to GND and the voltage of the T1 node is compared with GND by the comparator. In the differential circuit, GND is substituted for a common-mode voltage. Next, according to the comparator output, half of the 16 capacitors are connected to V_{REFP} or V_{REFN}. After it is repeated 4 times during Q_{SAR} phases, the 4b digital codes are stored in the first SAR logic. Finally, the feedback capacitors C_{F1} and C_{F2} are connected to the opamp output, and each capacitor of C_1 to C_{16} is individually connected to one of V_{REFP}, V_{REFN} or GND depending on the 4b codes in Q_{SAR} phases. The residue opamp transfers the residue voltage to the next stage.

B. Reference buffer with deglitch circuit

The proposed ADC uses the two reference buffers to improve the settling and accuracy of the reference voltages. Fig. 4 illustrates the reference buffer driving the channel1 of the proposed ADC. The deglitch circuit is based on deglitch switches of MPA, MPB, MNA, and MNB and a pulse generator. When reference switches connected to the bottom plates capacitors are turn on, the reference voltages make large peak in an instant and are settled to the required voltage level. To stabilize the reference voltages in a short time, conventional reference buffers dissipate the large static current

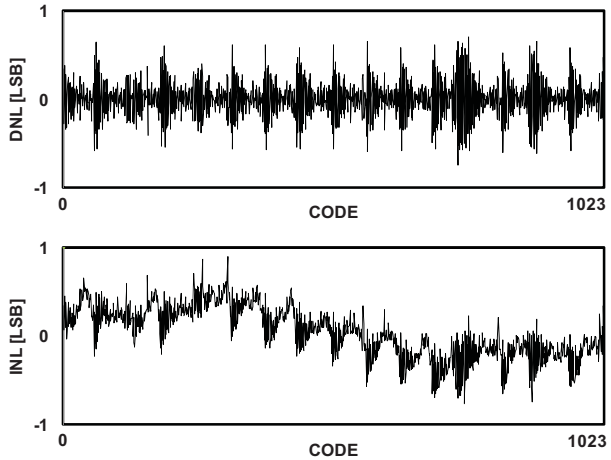

Fig. 6 Measured DNL and INL.

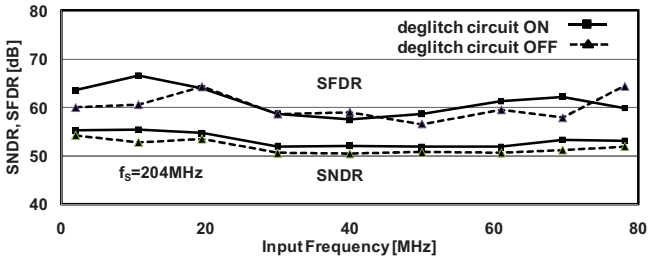

Fig. 7 Measured dynamic performance.

flowing through the R0. On the other hand, the reference buffer with the proposed deglitch circuit reduces the static current by mean of dynamic current control. Because the bit-decision signals are simultaneously generated with the digital output codes of the SAR ADCs, the reference glitches occur after the transition of the bit-decision signals. So, the control signals of PA1<3:0>, PB1<6:0>, NA1<3:0>, and NA1<6:0> with the fixed pulse width are simply made by the bit-decision signals. Therefore, the NMOS and PMOS switches are turned on to supply a large amount of charge to V_{REFP} and V_{REFN} at the point of the reference switching. The switches are connected to VDD or GND since the large peaks of the reference voltages occur in the direction of a common-mode voltage. The amount of charge supplied to the reference voltages is decided by the switch size and pulse width. The size of the deglitch switches is optimized depending on the capacitance.

IV. Measurement Results

The prototype pipelined SAR ADC is fabricated in a 65nm CMOS process with MOM capacitors as shown in Fig. 5. The active die area of the ADC is 0.22mm^2 (=0.85mm×0.26mm) with the reference buffer and the current generator. Fig.6 plots the measured differential nonlinearity (DNL) and integral nonlinearity (INL) at a 10b accuracy. The DNL and INL are ±0.74LSB and ±0.90LSB, respectively. Fig. 7 shows the measured dynamic performances versus the input frequency depending on the deglitch circuit. After the deglitch circuit is turned on as plotted in solid lines, the signal-to-noise-and-distortion ratio (SNDR) is improved around 1.3dB and the

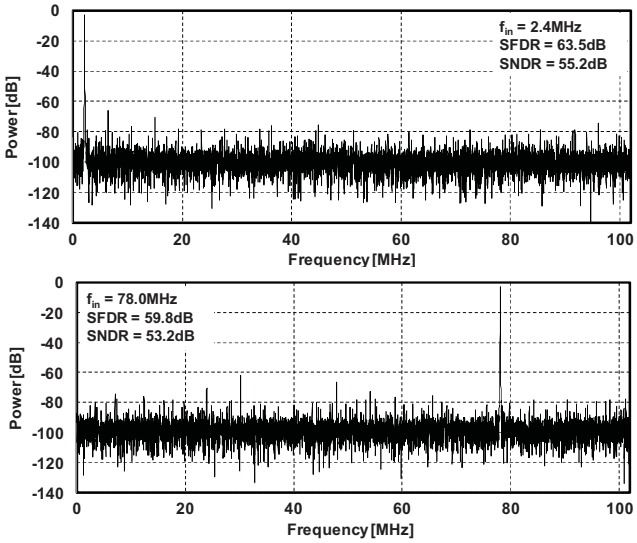

Fig. 8 Measured FFT plots.

TABLE I. ADC PERFORMANCE SUMMARY

Process	65nm 1P6M CMOS (MOM cap.)
Resolution	10 bit
Conversion Rate	204 MSample/s
Supply Voltage	1.0 V
Power Consumption	9.15 mW
DNL, INL	+0.71/-0.74 LSB, +0.90/-0.77 LSB
SNDR	55.2 dB @ f_{in}=2.4 MHz
SFDR	63.5 dB @ f_{in}=2.4 MHz
Active Die Area	0.22 mm^2 (= 0.85×0.26 mm^2)
FoM	95.4 fJ/conversion-step

TABLE II. 10BIT ADC PERFORMANCE COMPARISON

	[1]	[3]	[8]	[9]	[10]	This work
Fs (MS/s)	205	210	205	200	210	204
Supply (V)	1.0	1.8	1.2/3.3	1.2	1.2	1.0
SFDR (dB)	64.8	86	73.5	66.5	74	63.5
SNDR (dB)	55.2	59.4	56	54.4	55	55.2
Power (mW)	61	140	93	55	52	9.5
Area (mm^2)	1.0	1.5	0.52	1.26	0.38	0.22
Process (nm)	90	180	130	90	130	65
FoM (fJ/conv)	633	877	880	641	539	95.4

spurious-free dynamic range (SFDR) is equal or higher in most of the input frequencies. Fig. 8 shows the measured FFT plots of the ADC at a 204MHz sampling frequency. In a 2.4MHz input frequency, the SNDR is 55.2dB and the SFDR is 63.5dB. In the 78.0MHz input frequency, the SNDR and the SFDR are 53.2dB and 59.8dB, respectively. The total ADC power consumption is about 9.15mW at a 204MS/s with a 1.0V supply. The analog circuits including the reference buffers and the digital circuits dissipate 6.4mW and 2.75mW, respectively. The Figure of Merit (FoM) is defined as

$$FOM = P_{DISS} / (2^{ENOB} \times f_S) \quad (1)$$

where P_{DISS} is the power dissipation, ENOB is the effective number of bits, and f_S is the sampling frequency. From (1), the proposed ADC's FoM is 95.4fJ/conversion-step. The measured performance of the prototype ADC is summarized in Table I. Table II provides a comparison with other high speed 10b ADCs published in recent years. The proposed high-speed pipelined SAR ADC provides comparable area and FoM with maintaining the 10b performances.

V. CONCLUSION

This paper describes the pipelined SAR ADC employing dual-channel architecture for small chip area and low power consumption. The amplification time is increased by the proposed asynchronous timing technique and the reference glitches are reduced by the deglitch circuit. The prototype ADC fabricated in a 65nm CMOS process occupies 0.22mm^2 and dissipates 9.15mW at a 204MSample/s and a 1.0V supply voltage.

ACKNOWLEDGMENTS

This work was supported by IT R&D program of MKE/IITA, Rep. of Korea (2008-S-015-01, Development of Analog Circuit Techniques for Mixed SoC based on 45nm CMOS Technology).

REFERENCES

[1] S.-C. Lee et al., "A 10-bit 205MS/s 1.0-mm^2 90-nm CMOS Pipeline ADC for Flat Panel Display Applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2688-2695, Dec. 2007.

[2] J. Li, et al., "A 10b 170MS/s CMOS Pipelined ADC Featuring 84dB SFDR without Calibration," *Symp. VLSI Circuits*, pp. 226-227, June 2006.

[3] J. R. Leboeuf et al., "A 1.8V 10b 210MS/s CMOS Pipelined ADC Featuring 86dB SFDR without Calibration," *CICC*, pp. 317-320, Sept. 2007.

[4] V. Giannini, et al., "An 820μW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," *ISSCC Dig. Tech. Papers*, pp. 238-239, Feb. 2008.

[5] C-C. Liu, et al., "A 10b 100MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation," *ISSCC Dig. Tech. Papers*, pp. 386-387, Feb. 2010.

[6] M. Furuta, M. Nozawa, and T. Itakura, "A 0.06mm^2 8.9b ENOB 40MS/s pipelined SAR ADC in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 382-383, Feb. 2010.

[7] S. M. Louwsma, et al., "A 1.35GS/s, 10b, 175 mW Time-Interleaved AD Converter in 0.13μm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, pp.778-786, Apr. 2008

[8] B. Hernes et al., "A 92.5mW 205MS/s 10b Pipeline IF ADC Implemented in 1.2V/3.3V 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 462-463, Feb. 2007

[9] D. Kurose et al., "55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp.1589-1595, July 2006.

[10] Z. Cao and S. Yan, "A 52mW 10b 210MS/s Two-Step ADC for Digital-IF Receivers in 0.13μm CMOS," *CICC*, pp. 309-312, Sept. 2008.